Remarks

By this amendment claims 1 and 16 have been amended. Claims 1 through 16 are pending, no new matter has been entered, and reconsideration thereof is requested.

Claim Rejections - 35 U.S.C. § 103

The Examiner rejected Claims 1,2, and 5 under 35 U.S.C.§ 103(a) as being unpatentable over Crafts (U.S. Patent No. 6,064,588) and Iizuka et al (U.S. Patent No. 4,641,165). The Examiner indicates that Crafts shows most aspects of the instant invention including first and second transfer devices and differential storage capacitor. The Examiner points out that Crafts does not show the primary capacitance of the storage capacitor being at least approximately 5 times the inherent capacitance of the said capacitance, but mentioned Iizuka, et al. teaches how to make a primary capacitor to be at least approximately 5 times the inherent capacitance. The Examiner concludes it would have been obvious to make the primary capacitance to be approximately 5 times the inherent capacitance.

The Applicants respectfully believe that the references do not show, or suggest, the present invention. Further, Iizuka, et al. do not teach a differential capacitance at least 5 times the inherent capacitances since Iizuka does not incorporate a differential capacitor. The Examiner indicated in his response to arguments that Iizuka et al is analagous to that shown in Crafts, however, as will be later pointed out, Crafts uses a different topology and two capacitors and does not concern himself with parasitic or inherent capacitances. No motivation appears in the cited references to produce the claimed invention, consider if one were to re-wire the capacitor of Crafts or Iizuka et al. in a different manner, it would not present the same invention nor size the

capacitor to be at least 5 times the inherent capacitance without further invention. Thus, the works of Crafts and Iizuka et al. taken together or individually would require further invention to identify a low-capacitance means of wiring the second capacitor node of Iizuka et al. differentially.

The Examiner acknowledges that "Crafts does not explicitly show the primary capacitance of the storage being at least approximately 5 times the inherent capacitance" and concludes that it would have been obvious to make it so. However, a closer inspection of the invention of Crafts reveals that is not reasonably possible for the work of Crafts to achieve such a ratio nor does Crafts use a single capacitor but in fact uses two capacitors 62c and 62d which totally avoids the problem of inherent capacitance. Our invention uses only one single differential capacitor CST to store charge and which connects two transistors T1 and T2 that is confronted with the inherent capacitance problem. Further, Crafts makes it clear by stating "each memory cell includes a logically complementary pair of charge storage capacitors which establish a data bit signal from each cell by a relative difference in charge stored on the capacitors." Our invention does not include a logically complementary pair of capacitors, but rather a single capacitor.

Furthermore, Crafts' pair of capacitors cannot be argued to be equivalent to our single capacitor. Crafts requires a three-terminal connection to the pair of capacitors (the third terminal being connected to element 63 in Crafts' Fig 1) while our invention teaches away from this concept,

allowing only two terminals, as a third terminal would make our invention inoperable. Thus the pair of capacitors in Crafts cannot be construed as equivalent to or teaching our invention.

Note that Crafts invention requires an auxiliary word-line (63 in Fig 1) to connect the third terminal of the capacitor pairs together. This is required to develop the differential bit signal as described in Crafts. By contrast, our invention has no auxiliary word-line as it does not have pairs of capacitors tied to a third terminal. Further, this connection defeats the purpose of our invention to reduce charge loss because in Crafts any charge loss in any one capacitor to a surrounding electrical node will discharge that particular capacitance with a return current through the connection, 63, thereby defeating the cancellation that is enjoyed by our invention. The Examiner stated in the response to Arguments that Crafts "teaching away" is not pertinent to the present invention because Crafts has a broader disclosure or non-preferred embodiments. This is not the case as stated above and our inventive structure is topologically distinct from that of Crafts, and uniquely possesses our claimed ability to substantially reduce differential charge loss. In the Crafts structure, any charge lost in any one capacitor is not offset in its differential complement, since the common lines connecting the return paths of the storage capacitors in Crafts will provide the discharge path. Even if Crafts leaves the return line "floating," the aggregate of all of the cells tied to this one node (63) act exactly as an inherent capacitance and are in aggregate much greater than the differential capacitance; hence the storage capacitance

must, in fact, be less than that of the inherent capacitance in the invention of Crafts. This difference underscores the novelty of our invention.

Iizuka provides an entirely different approach to charge storage from both our invention and that of Crafts. Iizuka uses a circuit topology distinct from Crafts, and application of the low-capacitance node to Crafts memory cell would make result in inherent capacitance that is still larger than the storage capacitance by virtue of the common connection in Crafts (63). Thus the teaching of Iizuka together with that of Crafts fails to achieve the desired result of our invention. Iizuka can keep the inherent capacitance low by virtue of the resistor isolation, "R" in Fig. 11, which when applied to the work of Crafts becomes defeated by the essential connection "63". Hence, the combination of these two works distinctly fails to lead to our invention.

Furthermore, neither work identifies the use of fully-depleted transfer devices that prevents differential charge loss which are the subject of Claims 1, 2, and 5 in order to enable the capacitance goals recited therein.

Based on the foregoing, it is respectfully submitted that Claims 1,2, and 5 are not obvious under 35 U.S.C.§103(a).

The Examiner rejected claims 3 and 4 under 35 U.S.C. 103(a) as being unpatentable over Crafts and Iizuka et al., as applied to Claim 1 above, and further in view of Tashiro (U.S. Patent No. 5,241,211).

Based on the above discussion, the invention of claims 1,2 and 5 should be allowable along with all dependent claims, accordingly claims 3, 4, and 6-15 should also be allowable.

The Examiner rejected claims 6 to 16 under 35 U.S.C.§103(a) as being unpatentable over Crafts and Iizuka et al., as applied to Claim 1 above, and further in view of Choi et al. (DRC 2000).

The Examiner indicated that Crafts and Iizuka et al. show most aspects of the instant invention except for the features of the transfer devices and the storage capacitor disposed on rails of semiconductor material. Choi et al. teach (e.g. Figure 1) to form semiconductor devices using semiconductor rails to reduce parasitic capacitance and resistance. The Examiner believes it would have been obvious to a person or ordinary skill in the art at the time of invention to form semiconductor devices using semiconductor rails as taught by Choi et al. in the device of Crafts and Iizuka et al. to reduce parasitic capacitance and resistance.

The Applicants point out again that Iizuka et al. and Crafts do not suggest the invention of Claim 1 or 16. Nor does Choi et al. teach or suggest the use of ultra-thin-body SOI to form and FET.

They do not contribute to the use of "rails" nor to using a single capacitance as a storage element with a two-terminal capacitive circuit. Instead, they employ a three-terminal pair of capacitors. Choi teaches a FinFET, with no indication of connection to capacitors by any means that avoid the problem of inherent capacitance that would accompany any ordinary means of interconnecting the structure of Choi to a storage element. Choi instead teaches a conventional interconnect with its associated (high) level of parasitic (and therefore intrinsic) capacitance. It would not be obvious to extend the length of the "fin" in Choi to provide a connection to a capacitor which is integral with the fin, as in our invention. Taking Choi with Crafts would lead to a pair of capacitors in an array with a third connection to an auxiliary work-line (63 of Crafts) and with planar capacitors with large inherent capacitance to the substrate.

The Examiner argues that Tashiro (US5,241,211) teaches use of an SI substrate to reduce capacitances thus it would be obvious to use SOI in the device of Crafts and Iizuka to reduce parasitic capacitances, however the parasitic capacitance, even on an SOI structure, would not meet our requirement for low inherent capacitance. Firstly, the connection of the third capacitor-pair terminals in Crafts would immediately negate the claim as charge would flow through this third terminal (63 of Crafts Fig. 1) even on an SOI substrate, and in Iizuka there is no provision whatsoever for differential charge storage, and hence SOI would provide no benefit. In our invention a semiconductor rail which is shared both by the transfer devices and the storage capacitor, is able to provide a unique structure that enables the single, two-terminal capacitance

between the two rails, almost exclusively (ie, negligible intrinsic capacitance) and without a source of charge loss in a third terminal (such as 63 in Crafts).

Based on the foregoing, it is submitted that Claims 6 to 16 are not obvious under 35 U.S.C.§103(a).

Conclusion

Based on the foregoing, it is respectfully submitted that all the claims active in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,

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